CLAIMS

1. A method for multiplexing data from a plurality of input channels that can differ in data phase and/or bit rate into a serial signal, comprising the steps of:

storing the data, respectively arriving from the plurality of input channels, into separate memories respectively; and

retrieving the data from the respective memories in a predetermined order, and multiplexing the data, together with timing data indicating the presence of the data, into a serial signal of a frame structure having time slots fixedly assigned to the respective input channels.

2. A method according to claim 1, wherein a plurality of first bit storing positions and the same number of second bit storing positions are assigned for one bit of data, and the same value as the value of the data is stored in each of the plurality of first bit storing positions while, in the plurality of second bit storing positions, timing data whose value changes is stored when the data exists, but timing data whose value does not change is stored when the data does not exist.

3. A method according claim 2, wherein

the data from the plurality of input channels are order wire data from a plurality of communication lines, and

the serial signal having the frame structure consists of a single serial signal, and wherein

the data are multiplexed in such a manner that respective ones of the plurality of first bit storing positions and respective ones of the plurality of second bit storing positions appear on the serial signal at intervals equal to an integer multiple of the number of input channels.

4. A method according claim 2, wherein

the data from the plurality of input channels are data communication channel data from a

plurality of communication lines, and

the serial signal having the frame structure consists of a first serial signal for carrying the data and a second serial signal for carrying the timing data, and wherein

the data are multiplexed in such a manner that respective ones of the plurality of first bit storing positions and respective ones of the plurality of second bit storing positions appear on the first serial signal and the second serial signal, respectively, at intervals equal to the number of input channels.

5. A multiplexing apparatus for multiplexing data from a plurality of input channels that can differ in data phase and/or bit rate into a serial signal, comprising:

a plurality of memories for separately storing the data respectively arriving from the plurality of input channels; and

a multiplexing block for retrieving the data from the respective memories in a predetermined order, and for multiplexing the data, together with timing data indicating the presence of the data, into a serial signal of a frame structure having time slots fixedly assigned to the respective input channels.

6. An apparatus according to claim 5, wherein a plurality of first bit storing positions and the same number of second bit storing positions are assigned for one bit of data, and the same value as the value of the data is stored in each of the plurality of first bit storing positions while, in the plurality of second bit storing positions, timing data whose value changes is stored when the data exists, but timing data whose value does not change is stored when the data does not exist.

7. An apparatus according to claim 6, wherein

the data from the plurality of input channels are order wire data from a plurality of communication lines, and

the serial signal having the frame structure consists of a single serial signal, and wherein

the data are multiplexed in such a manner that respective ones of the plurality of first bit storing positions and respective ones of the plurality of second bit storing positions appear on the serial signal at intervals equal to an integral multiple of the number of input channels.

8. An apparatus according claim 6, wherein

the data from the plurality of input channels are data communication channel data from a plurality of communication lines, and

the serial signal having the frame structure consists of a first serial signal for carrying the data and a second serial signal for carrying the timing data, and wherein

the data are multiplexed in such a manner that respective ones of the plurality of first bit storing positions and respective ones of the plurality of second bit storing positions appear on the first serial signal and the second serial signal, respectively, at intervals equal to the number of input channels.